

### REMARKS

Claims 1, 3-53 are currently pending in the subject application and are presently under consideration. Claim 3 has been amended herein to further emphasize various distinguishing features. A listing of the pending claims can be found at pages 2-9 of this Reply.

Favorable reconsideration of the subject patent application is respectfully requested in view of the amendments and comments herein.

#### **I. Rejection of Claim 1 Under 35 U.S.C. §112, First Paragraph**

Claim 1 stands rejected under 35 U.S.C. §112 as failing to comply with the written description requirement. Withdrawal of this rejection is respectfully requested for at least the following reasons. The specification discloses in full, clear, concise, and exact terms that which can enable one to carry out the claimed subject matter.

At page 3 of the Office Action (mailed July 5, 2007), the Examiner contends that there is no disclosure within the specification or original claims for a time synchronization apparatus that “is configurable to operate as both a synchronization master and a synchronization slave” as recited in independent claim 1. In particular, the Examiner contends the disclosure provides for acting as **either** a master **or** a slave, but not **both** a master and a slave **at the same time**.

Applicants’ representative respectfully points out that the Examiner is misreading the claim. Claim 1 does not articulate that the time synchronization apparatus **acts** as both a master and a slave at the same time, but rather that “the time synchronization apparatus **is configurable** to operate as both” a master and a slave, which is precisely what the specification notes in numerous locations. For example, the time synchronization apparatus can be configured to operate as a master, and at the same time can also be configured to operate as a slave. (*See e.g.*, pg. 37, ll. 9-11). Whether the apparatus is ultimately configured as a master or a slave is irrelevant, but it should be underscored that the apparatus can be configurable for both. Moreover, the synchronization apparatus can act as both a master and a slave, such as when operating as a local master in one time zone but operating as a slave to the global master. (*See* pg. 17, ll. 1-10).

In essence, the Examiner freely admits that there is support for a broader claim such as a time synchronization apparatus that is configurable as either a master or a slave, yet incongruously argues there is no support for a claim with identical subject matter, but that is

necessarily narrower in scope (*e.g.*, an apparatus that is configurable as both a master and a slave has a narrower scope than one that is configured as one or the other). More generally, if the specification states that an apparatus can be configurable as A or configurable as B, then inherently, the apparatus can be configurable as both A and B, yet requiring the apparatus to be configurable as both, narrows the scope over allowing it to be configurable as either A or B. The specification discloses in full, clear, concise, and exact terms the aforementioned features. (*See e.g., Id.*). Accordingly, this rejection should be withdrawn.

## **II. Rejection of Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 Under 35 U.S.C. §103(a)**

Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, *et al.* (US 4,807,259, hereinafter referred to as “Yamanaka”) in view of Voth (US 6,199,169). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Neither Yamanaka nor Voth, either alone or when combined, disclose all the claimed features. Moreover, Yamanaka and Voth produce an inoperative combination and are therefore not permissibly combinable.

*If references taken in combination would produce a "seemingly inoperative device," we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness. In re Spinnoble, 405 F.2d 578, 587, 160 USPQ 237, 244, 56 C.C.P.A. 823 (1969) (references teach away from combination if combination produces seemingly inoperative device); see also In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (inoperable modification teaches away). McGinley v. Franklin Sports Inc., 262 F.3d 1339, 60 USPQ2d 1001, 1010 (Fed. Cir. 2001) (emphasis added).*

The claimed subject matter relates generally to industrial control systems (*see, e.g.*, control system 50, FIG. 2) with a time synchronization apparatus (*see, e.g.*, S/L 82, FIG. 2) for synchronizing operation of a first controller (*see, e.g.*, controller 56, FIG. 2) with that of a second controller (*see, e.g.*, controller 54, FIG. 2). More specifically, the time synchronization apparatus can be configured to operate as either a master or a slave (and therefore can be configurable as both), can synchronize across disparate and/or multiple time synchronization zones (*see e.g.*, pg. 12, line 15 – pg. 14, line 26) and can function in topologies other than a star

topology such as a daisy chain or loop configuration, or combinations thereof (*see e.g.*, pg. 18, ll. 15-17). In particular, independent claim 1 recites, “a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is ***configurable to operate as both a synchronization master and a synchronization slave.***” Similarly, independent claims 38 (and similarly claim 39 and 52) recites, “a synchronization circuit...***configurable*** by the host.” Yamanaka does not disclose such features.

Yamanaka relates to a time synchronization method, wherein the time of a slave clock is synchronized with the time of a master clock. (*See* col. 7, ll. 6-49). The master clock resides in a master station (*see* element 17, FIG. 3A) and the slave clock resides in a slave station (*see* element 37, FIG. 3B). While Yamanaka discloses a method for time synchronization for a slave clock, the reference is silent as to whether either the master or the slave station is configurable. Accordingly, Yamanaka does not teach a time synchronization apparatus that is ***configurable to operate as both a synchronization master and a synchronization slave.*** Rather, Yamanaka teaches a designated master station that synchronizes a designated slave station.

At page 4 of the Office Action, the Examiner incorrectly argues Yamanaka teaches these features by suggesting two mutually exclusive scenarios. In the first case, the Examiner argues that the master station (or components thereof) is the synchronization apparatus to illustrate that the apparatus is a master, while in the second case, the Examiner argues the slave station is the synchronization component to stand for the proposition that the apparatus is a slave. Such analysis ignores the claimed features that the apparatus is configurable as both a master and a slave in favor of showing that both a master and a slave can exist independently in a system, which does not read upon the claims. Moreover, the Examiner has failed to identify which feature of Yamanaka is the synchronization apparatus of the subject claims, pointing instead to multiple distinct (and independent) elements of the reference to represent a single component of the claims. If the Examiner suggests the synchronization apparatus is the master station (or components thereof) then it is readily apparent that the reference does not teach “configurable to operate as ... a synchronization slave.” Likewise, if the synchronization apparatus is to be the slave station (or components), a similar deficiency exists. The Examiner is not free to change the definition of the apparatus in order to reject the claim piecemeal. Moreover, in either case, Yamanaka does not contemplate a time synchronization apparatus that is ***configurable.***

Accordingly, the Examiner has failed to present a *prima facie* case for obviousness and this rejection should be withdrawn.

Moreover, the Examiner seeks to combine Yamanaka with Voth, yet such a combination would produce a seemingly inoperative device. The method for time synchronization disclosed in Voth relies upon the assumption that the round-trip time between master and slave (transmission delay or latency) is zero. Hence, the accuracy of the method disclosed in Voth is a function of the speed of the network (*see e.g.*, col. 8, ll. 57-58), thus Voth is suitable for a SSI computer clusters as disclosed, but is wholly inapplicable to industrial control system networks such as that of Yamanaka. In contrast, Yamanaka calculates the transmission delay,  $\tau_1$ , (by averaging the round-trip times) in order to perform synchronization (*see* col. 7, line 32), which is impossible as applied to Voth, since Voth does not teach referencing round-trip times, but merely assumes this factor is always zero. Accordingly, the combination of Yamanaka and Voth would produce a seemingly inoperative device, which cannot therefore stand as predicates for a *prima facie* case for obviousness. Hence, for yet another reason, the Examiner has failed to present a *prima facie* case for obviousness and this rejection should be withdrawn for yet another reason.

#### ***Claims 4-6 and 15-17***

Claims 4 and 15 recite a transmitter that periodically transmits message frames at a fixed period of 50 $\mu$ s. Voth clearly does not teach this limitation. Rather, Voth merely indicates that messages can be transmitted at fixed intervals, but does not disclose any specific interval, much less one that is 50 $\mu$ s. The Examiner is not free to ignore the claimed features of 50 $\mu$ s simply because the specification suggests other intervals are also possible. The claims do not say “or some other fixed period.” Instead, the claims state 50 $\mu$ s. Voth does not.

Similarly, claims 6 and 17 recite a transmitter transmits a message frame having an LCM indicator at a least common multiple of 600ms. It is readily apparent that Voth does not teach 600ms. Again, the Examiner ignores the plain language of the claim because the specification teaches one in the art that other times can exist. Moreover, regarding claims 5 and 16 (*et al.*), Voth cannot even have an LCM interval at all given that latency is assumed to be zero. The Examiner’s arguments to the contrary do not appear to relate to the claims in any fashion. In addition, the Examiner is reminded that “the examiner should always look for enabled, allowable

subject matter and communicate to applicant what that subject matter is at the earliest point possible in the prosecution of the application.” (See MPEP § 2164.04) (underline in original).

### ***Claim 53***

Neither Voth nor Yamanaka teach the synchronization apparatus exists in a different synchronization time zone from that of the host processor as recited in dependent claim 53. At page 24 of the Office Action, the Examiner argues to the contrary citing Voth at col. 4, ll. 17-19 and suggesting that “distributed internetworking environment such as the Internet operates across time zones.” Be that as it may, such a statement has nothing whatever to do with Voth. Neither at the indicated portions nor anywhere else does Voth teach these features. Rather, Voth is expressly indicated to operate in a high speed TNet, which is not the Internet. Voth cannot function if the network were the Internet due to a latency that would render the method of Voth worthless, as any latency that is greater than half a clock cycles makes Voth inoperable. (See col. 8, ll. 60-66).

### **III. Rejection of Claims 8-12 Under 35 U.S.C. §103(a)**

Claims 8-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, in view of Voth and Ramussen, *et al.* (US 6,449,732, hereinafter referred to as “Ramussen”). Withdrawal of the rejection is respectfully requested because Yamanaka, Voth, and Ramussen, *et al.*, either alone or in combination with one another, do not teaches the all the claimed features.

In particular, claims 8-12 depend directly or indirectly upon independent claim 1. As noted *supra*, the cited references do not teach or suggest applicants’ invention recited in the subject claims. Ramussen, *et al.* fails to make up for the aforementioned deficiencies of Yamanaka and Voth with respect to independent claim 1. Thus, this rejection should be withdrawn.

### **IV. Rejection of Claims 29, 35-37, and 47 Under 35 U.S.C. §103(a)**

Claims 29, 35-37, and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Voth and in further view of Kuribayashi, *et al.* (US. 6,775,246, hereinafter referred to as “Kuribayashi”). Withdrawal of the rejection is respectfully requested

for at least the following reasons. Yamanaka, Voth, and Kuribayashi all fail to teach the all features of the claims, either alone or in combination with one another.

Claims 29, 35-37 depend directly or indirectly upon independent claim 1 while claim 47 depends directly or indirectly upon independent claim 39. As noted *supra*, the Yamanaka and Voth fail to teach or suggest all aspects of the subject claims. Kuribayashi fails to make up for the aforementioned deficiencies with respect to independent claims 1 and 39. Thus, this rejection should be withdrawn.

**Conclusion**

The present application is believed to be in condition for allowance in view of the above amendments and comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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